IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Original): A COC device comprising:

a logic chip having a logic circuit;

a memory chip mounted on the logic chip, the memory chip comprising: basic chips functioning as a chip independently from each other; and a dicing line interposed between the basic chips, connecting the basic chips, and configuring a part of the memory chip; and

a bump connecting the logic chip and the memory chip.

Claim 2 (Original): The COC device according to claim 1, wherein the basic chips have all the same layout.

Claim 3 (Previously Presented): The COC device according to claim 1, wherein at least a first portion of the basic chips has a layout that is inverted with respect to a layout of a second portion of the basic chips.

Claim 4 (Currently Amended): The COC device according to claim 1, ~~wherein the dicing line is formed with~~ further comprising at least one of an alignment mark and a test element group provided in the dicing line.

Claim 5 (Original): The COC device according to claim 1, wherein in the case where the basic chips are square, one side of individual basic chips has a length of 2 mm or more.

Claim 6 (Original): The COC device according to claim 5, wherein the dicing line has a width of 0.1 mm.

Claim 7 (Original): The COC device according to claim 1, wherein the basic chips have a bump.

Claim 8 (Original): The COC device according to claim 1, wherein the basic chips have a circuit capable of changing a word organization by a control signal.

Claim 9 (Currently Amended): A COC device comprising:

a logic chip having a logic circuit;

a memory chip mounted on the logic chip, the memory chip comprising: basic chips functioning as a chip independently from each other, and ~~capable of~~ changing a ~~word organization~~ specification of each basic chip by a control signal; and a dicing line interposed between the basic chips, connecting the basic chips, and configuring a part of the memory chip; and

a bump connecting the logic chip and the memory chip;

wherein the control signal is supplied from the logic chip to the memory chip.

Claim 10 (Original): The COC device according to claim 9, wherein the basic chips have all the same layout.

Claim 11 (Previously Presented): The COC device according to claim 9, wherein at least a first portion of the basic chips has a layout that is inverted with respect to a layout of a second portion of the basic chips.

Claim 12 (Currently Amended): The COC device according to claim 9, ~~wherein the dicing line is formed with~~ further comprising at least one of an alignment mark and a test element group provided in the dicing line.

Claim 13 (Original): The COC device according to claim 9, wherein in the case where the basic chips are square, one side of individual basic chips has a length of 2 mm or more.

Claim 14 (Original): The COC device according to claim 13, wherein the dicing line has a width of 0.1 mm.

Claim 15 (Original): The COC device according to claim 9, wherein the basic chips have a bump.

Claim 16 (Original): A SiP device comprising:

a COC device according to claim 1; and

a package covering said COC device.

Claim 17 (Original): A SiP device comprising:

a COC device according to claim 9; and

a package covering said COC device.

Claim 18 (New): The COC device according to claim 9, wherein the specification is a word organization of the basic chip.

Claim 19 (New): The COC device according to claim 9, further comprising a flash memory chip mounted on the logic chip, wherein the memory chip having the basic chips is a DRAM chip.

Claim 20 (New): The COC device according to claim 9, further comprising a DRAM chip mounted on the logic chip, wherein the memory chip having the basic chips is a flash memory chip.